ABSTRACT

The present invention is a memory circuit, comprises: a memory cell array including a plurality of bit lines, a plurality of word lines, and a plurality of memory cells disposed in the positions of intersection between the bit lines and the word lines; and a page buffer, which is connected to the bit line and which detects memory cell data by judging with predetermined sense timing the potential of the bit line when a pre-charged bit line potential is discharged in accordance to a cell current of a selected memory cell. Further the sense timing differs in accordance with the position of the selected memory cell in the memory cell array.